UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,244	03/21/2001	David Glen Roe	70803	2001

26327 7590 07/17/2002

THE LAW OFFICE OF KIRK D. WILLIAMS
1234 S. OGDEN ST.
DENVER, CO 80210

EXAMINER
COX, CASSANDRA F

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/814,244	Applicant(s) ROE, DAVID GLEN	
	Examiner Cassandra Cox	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 is indefinite because the phrase "designing a circuit" is unclear. It does not appear to the examiner upon examination of the specification that the applicant actually discloses a method for designing a circuit, but rather a method for providing a circuit that generates a first and a second clock reference signal. Correction or clarification is required.

Claims 16 and 17 are also rejected due to the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art "Phase-Locked Loop," ASIC SA-27 Databook, Document

No. SA 14-2214-02, IBM Corp., August 24, 1999, pp. 825-866 in view of Ho (U.S. Patent No. 6,240,152).

In reference to claim 1, applicant's admitted prior art (IBM reference) discloses on page 829 a first phase-locked loop circuit (PLL7SLIBE) including: an off-chip reference clock input (REFCLK), a first set of one or more phase-locked loop clock outputs (PLLOUTA, PLLOUTB, PLLOUTC), and a buffered reference clock output (BUFREFCLK); and a second phase-locked loop circuit (PLL7SLIBI) including: an on-chip reference clock input (REFCLK), a second set of one or more phase-locked loop clock outputs (PLLOUTA, PLLOUTB, PLLOUTC). The IBM reference does not disclose that the buffered reference clock output (BUFREFCLK) of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input (REFCLK) of the second phase-locked loop circuit (PLL7SLIBI). Ho discloses in column 1, lines 23-27 that it is well known in the art that phase-locked loops can be used by microprocessors to generate on-chip clock signals. Therefore, it would have been obvious to one of skill in the art at the time of the invention that the first phase-locked loop circuit (PLL7SLIBE) of the IBM reference could have been used to provide the on-chip reference clock to the second phase-locked loop circuit (PLL7SLIBI) as supported by the disclosure of Ho. The same applies to claims 9, 15, 18, and 20.

In reference to claim 2, the IBM reference discloses that the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit (PLL7SLIBE) includes at least two phase-locked loop clock outputs (PLLOUTA, PLLOUTB, PLLOUTC). The same applies to claim 10.

In reference to claim 3, the IBM reference further includes in Figure 23 a buffer (BUF) internal to the first phase-locked loop circuit, the buffer (BUF) being electrically connected between the off-chip reference clock input (REFCLK) and the buffered reference clock output (BUFREFCLK). The same applies to claim 17.

In reference to claim 4, the IBM reference discloses that the first phase-locked loop circuit (PLL7SLIBE) and the second phase-locked loop circuit (PLL7SLIBI) are predefined library circuits (which is seen to be the same as being defined as Macros). The same applies to claims 6, 7, 11, and 13.

In reference to claim 5, the IBM reference discloses on page 827 that the first phase-locked loop circuit (PLL7SLIBE) and the second phase-locked loop circuit (PLL7SLIBI) can be included in ASICs. The same applies to claims 12, 16, and 19.

In reference to claim 8, the IBM reference discloses on page 829 (in the Notes section) that the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad (I/O pads) of a chip. The same applies to claim 14.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-

872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TUAN T. LAM
PRIMARY EXAMINER

CC

July 12, 2002